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CMOS: Circuit Design, Layout, and Simulation: R. Jacob ...

R. JACOB (JAKE) BAKER, PhD, is an engineer, educator, and inventor. He has more than twenty years of engineering experience and holds more than 200 granted or pending patents in integrated circuit design. Jake is the author of several circuit design books for Wiley-IEEE Press. In 2007, he received the Hewlett-Packard Frederick Emmons Terman Award.

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R. Jacob (Jake) Baker is an engineer, educator, and inventor. He has more than twenty years of engineering experience and holds over 200 granted or pending patents in integrated circuit design. Jake is the author of several circuit design books for Wiley-IEEE Press. A more detailed biography is provided at the book's Web site.

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About The Author. R. JACOB (JAKE) BAKER, PhD, is an engineer, educator, and inventor. He has more than twenty years of engineering experience and holds more than 200 granted or pending patents in integrated circuit design.

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**(12) United States Patent (10) Patent N0.2 US 7,733,262 B2 ...**

US007733262B2 (12) United States Patent (10) Patent N0.2 US 7,733,262 B2 Baker (45) Date of Patent: \*Jun. 8, 2010 (54) QUANTIZING CIRCUITS WITH VARIABLE 6,781,906 B2 8/2004 Perner et al.

**United States Patent - CMOSedu.com**

US 6,809,981 B2 1 WORDLINE DRIVEN METHOD FOR SENSING DATA IN A RESISTIVE MEMORY ARRAY BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to the reading of resistor

**DESIGN OF A HIGH FREQUENCY AND LOW POWER SUCCESSIVE ...**

Abstract. In this paper, we present the design of a high frequency and low power analog to digital converter (ADC) which operates at 3V power supply using 1smc 0.18micron CMOS technology.

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R. JACOB (JAKE) BAKER, PhD, is an engineer, educator, and inventor. He has more than twenty years of engineering experience and holds more than 200 granted or pending patents in integrated circuit design.

**(PDF) A Fast-Locking Digital Phase-Locked Loop**

A conventional digital phase-locked loop (DPLL) is designed using (Baker et al., 2003) to operate at 1GHz using 0.18 um CMOS technology; its lock time is 4.19 mus.

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An important continuation to CMOS: Circuit Design,

Layout, and Simulation The power of mixed signal circuit designs, and perhaps the reason they are replacing analog only designs in the implementation of analog interfaces, comes from the marriage of analog circuits with digital signal processing.